IFW AF $

CERTIFICATE OF MAILING

I hereby certify that the below listed items are being deposited with the U.S. Postal Service as first class mail in an envelope addressed to:

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

on 09/21/04.

Marianne Boland

Marianne Boland

In Re Application of:

Bremer, et al.

Serial No.: **09/645,206**

Filed: **08/25/2000**

Confirmation No.: **4403**

Group Art Unit: **2643**

Examiner: **Barnie, Rexford N.**

Docket No.: **061607-1300**

For: **System And Method For Premises End Crosstalk Compensation**

The following is a list of documents enclosed:

Return Postcard
Transmittal of Appeal Brief
Fee Transmittal
Appeal Brief
Charge Deposit Account No. 16-0255 in the amount of $330.00

Further, the Commissioner is authorized to charge Deposit Account No. 16-0255 for any additional fees required. The Commissioner is requested to credit any excess fee paid to Deposit Account No. 16-0255.

TRANSMITTAL OF APPEAL BRIEF	Docket No. (Optional): **061607-1300**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Mail Stop Appeal Brief; Commissioner for Patents, P.O. Box 1450, Alexandria , VA 22313-1450 on

09/21/04

Marianne Boland

Signature – Marianne Boland

In re Application of **Bremer, et al.**	
Application Number **09/645,206**	Filed **08/25/2000**
For **System And Method For Premises End Crosstalk Compensation**	
Group Art Unit **2643**	Examiner **Barnie, Rexford N.**
Confirmation No.: **4403**	

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on 07/21/2004

The fee for this Appeal Brief is (37 CFR 1.17(c) $ 330.0

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.17(a)-(d) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

☐	One month (37 CFR 1.17(a)(1))	$ 110.0
☐	Two months (37 CFR 1.17(a)(2))	$ 420.0
☐	Three months (37 CFR 1.17(a)(3))	$ 950.0
☐	Four months (37 CFR 1.17(a)(4))	$ 1,480.0

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that the applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Method of Payment:

☒ Payment is enclosed as follows:

☐ A check in the amount of enclosed.

☐ Payment by credit card. Form PTO-2038 is attached in the amount of $_____.

☒ The Commissioner is authorized to charge 16-0255 to a Deposit Account $330.00.

☒ The Commissioner is hereby authorized to charge any deficiencies in fees, or credit any overpayment to Deposit Account No. 16-0255. A duplicate copy is enclosed.

Warning: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

September 21, 2004
Date

Raymond W. Armentrout

Raymond W. Armentrout

PTO/SB/17 (10-03)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revisions.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete If Known	
Application Number	09/645,206
Filing Date	08/25/2000
First Named Inventor	Bremer
Examiner Name	Barnie, Rexford N.
Group / Art Unit	2643
Attorney Docket No.	061607-1300

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit Card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account

Deposit Account Number: 16-0255

Deposit Account Name: Paradyne Corporation

The Commissioner is authorized to: *(check all that apply)*

☒ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) during the pendency of this application

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility Filing Fee	
1002	340	2002	170	Design Filing Fee	
1003	530	2003	265	Plant Filing Fee	
1004	770	2004	385	Reissue Filing Fee	
1005	160	2005	80	Provisional Filing Fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee From Below		Fee Paid
Total Claims		- 20**=		X 9.00 =	
Independent Claims		- 3** =		X 43.00 =	
Multiple Dependent				145.00 =	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	**Reissue independent claims over original patent
1205	18	2205	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

***or number previously paid, if greater; For Reissues, see above*

FEES CALCULATION *(continued)*

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge-late filing fee or oath	
1052	50	2052	25	Surcharge-late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive-unavoidable	
1453	1,330	2453	655	Petition to revive-unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee for provisional application	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	770	2810	385	For each add. invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited exam. of a design application	
				Other fee (specify)	

SUBTOTAL (3) ($) 330.00

*Reduced by Basic Filing Fee Paid

SUBMITTED BY

Complete (if applicable)

Typed or Printed Name	Raymond W. Armentrout	Registration No. 45,866	Telephone Number	770-933-9500
Signature	Raymond W Armentrout		Date	September 21, 2004

WARNING: Information on this form may become public. Credit Card Information should not Be Included on this form. Provide credit card information and authorization on PTO-2038

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:	)	
	)	
Bremer et al.	)	Art Unit: 2643
	)	
Serial No.: 09/645,206	)	Examiner: Barnie, Rexford N.
	)	
Filed: 08/25/2000	)	Docket No. 061607-1300
	)	
For: System and Method for Premises End Crosstalk Compensation	)	Appeal No.: _____
	)	
	)	

APPEAL BRIEF UNDER 37 C.F.R. §1.192

Mail Stop: Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the decision of Examiner Rexford N. Barnie in Group Art Unit 2643, of April 2, 2004, rejecting claims 1-65 in the present application and making the rejection Final.

I. REAL PARTY IN INTEREST

The real party in interest of the instant application is Paradyne Corporation, having its principal place of business at 8545 126th Avenue, North, Largo, Florida, 33773, as embodied in assignment recorded at Reel/Frame 011041/0036.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences or judicial proceedings so related to the present application that the outcome of them would impact or affect the outcome of this appeal.

III. STATUS OF THE CLAIMS

Claims 1-65 are currently pending in the application. This appeal is directed to the rejection of claims 1-65. More specifically, the Final Office Action mailed April 2, 2004, rejected claims 1-65 under 35 U.S.C. §103(a) as allegedly being unpatentable over Admitted prior art (Fig. 2) in view of *Sciacero et al.* (U.S. Patent 5,502,391), or *Arnett et al.* (U.S. Patents 6,186,834 or 6,176,742) and further in view of *Agazzi et al.* (U.S. Patent 4,669,116).

Applicants appeal the rejection of claims 1-65. For the reasons set forth herein, the Applicants respectfully submit that the rejection of pending claims 1-65 should be overturned by the Board of Patent Appeals.

IV. STATUS OF AMENDMENTS

No amendments have been made after the issuance of the Final Office Action, and amendments submitted before the issuance of the Final Office Action have been entered. A copy of the current claims is attached hereto as Appendix A.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

A. Concise Summary

Embodiments employ compensating capacitive devices coupled between a first pair of conductors (lines 1 and 2) and a second pair of conductors (lines 3 and 4) to reduce premises end crosstalk (PEXT) by providing an improved match between mutual coupling capacitances between the first wire pair (lines 1 and 2) and the second wire pair (lines 3 and 4). (For example, see the Summary of the Invention at page 10, line 14 through page 11, line 27).

B. Summary of the Invention as defined by Independent Claim 1.

> 1. A system for reducing undesirable signals in a communication network, comprising:
>
> means for compensating, said compensating means providing capacitance;
>
> means for connecting said compensating means to a pair of conductors selected from a plurality of conductors; and
>
> means for selectively actuating said compensating means such that said compensating means, when actuated by said actuating means, reduces an undesirable crosstalk signal caused by a mismatch between a plurality of mutual capacitive couplings associated with said plurality of conductors.

In this embodiment, compensating means are connected to a pair of conductors selected from a plurality of conductors by a means for connecting, such that a means for compensating provides capacitance. When the means for selectively actuating actuates the compensating means, the compensating means reduce an undesirable crosstalk signal caused by a mismatch between a plurality of mutual capacitive couplings associated with said plurality of conductors.

The structure of a "***means for compensating, said compensating means providing capacitance***" is illustrated generally in figure 4 as the crosstalk compensator 200, which is described with particularity in the Specification at page 14, line 8 through page 15, line 16.

Structure of a more specific embodiment is illustrated in figures 5 and 6 (reference numeral 200), and is described with particularity in the Specification at page 15, line 19 through page 21, line 24. Other embodiment structures are disclosed in: figure 7 (reference numeral 201, described with particularity in the Specification at page 21, line 27 through page 23, line 17); figure 8 (reference numeral 202, described with particularity in the Specification at page 23, line 20 through page 24, line 23); figure 9 (reference numeral 203, described with particularity in the Specification at page 24, line 26 through page 25, line 31); figure 10 (reference numeral 204, described with particularity in the Specification at page 26, lines 6-31); figure 11 (reference numeral 205, described with particularity in the Specification at page 27, line 6 through page 28, line 20); figure 12 (reference numeral 206, described with particularity in the Specification at page 28, line 23 through page 30, line 7); and figure 13 (reference numeral 207, described with particularity in the Specification at page 30, line 10 through page 31, line 9). In the above-described embodiments, these means provide the capacitance.

The structure of a "***means for connecting said compensating means to a pair of conductors selected from a plurality of conductors***" for the above-described embodiments are illustrated in the figures 4-12 by the connections made to lines 1 and 2 with lines 3 and 4 (and/or lines *m* and *n* in the embodiment of figure 13, described below). An exemplary description of the means for connecting is provided in the Specification at page 20, line 23 through page 21, line 24. Other examples are described in the Specification at: page 21, line 27 through page 22, line 34; page 23, line 31 through page 24, line 23; page 24, lines 29-31; and elsewhere. In the above-described embodiments, these means provide the connectivity to the pairs of conductors (lines 1 and 2 with lines 3 and 4).

The structure of a "***means for selectively actuating said compensating means***" for the above-described embodiments are illustrated in the figures 6-12 by the switching devices. In figure 6, switches S1-S6 are illustrated and are described with particularity in the Specification at page 20, lines 7-22. In figure 7, switches S1-S3 and connection points 210 and 216 are illustrated and are described with particularity in the Specification at page 22, line 7 through page 23, line 17. In figure 8, switches S1-S3, SA and SB are illustrated and are described with particularity in the Specification at page 23, line 31 through page 24, line 15. In figure 9, switches S1-S3 and processor based switch 250 are illustrated and are described with particularity in the Specification at page 24, line 31 through page 25, line 24. In figure 10, CC switcher 266 and line switcher 264 residing in the processor based switch 260 are illustrated and are described with particularity in the Specification at page 26, lines 6-22. In figure 11, CC switcher 276, line switcher 274 and detector 278 residing in the processor based switch 270 are illustrated and are described with particularity in the Specification at page 27, line 7 through page 28, line 9. In figure 12, three-way switches 288 and 290 residing in the first CC switcher 284 and the second CC switcher 286, respectively, and the detector 288 (which all reside in the processor based detector and switch 280) are illustrated and are described with particularity in the Specification at page 28, line 23 through page 29, line 21. In figure 13, capacitor compensating switches 310 and 312 residing in the first CC switcher 304 and the second CC switcher 306, respectively, and the detector 308 (which all reside in the processor-based detector and switch 300) are illustrated and are described with particularity in the Specification at page 30, lines 10-33. In the above-described embodiments, these means provide the selectivity.

The act in the above-described "***means for selectively actuating said compensating means***" for the above-described embodiments are performed manually by the installer (in the

embodiments identified by reference numerals 200, 201 and 202 in figures 6-8, respectively) or automatically by the processor based switches 250, 260, 270, 280 or 300 (figures 9-13, respectively).

C. Summary of the Invention as defined by Independent Claim 33.

> 33. A system for reducing undesirable signals in a communication network, comprising:
> a plurality of compensating capacitive devices;
> a plurality of switches, each uniquely coupled to one of said capacitive devices; and
> a processor controlling said switches,
> such that when at least one of said switches are actuated by said processor, said corresponding compensating capacitive device is connected between two conductors of a four conductor system, such that said compensating capacitive device reduces an undesirable crosstalk signal caused by a first mismatch between a plurality of mutual capacitive couplings associated with said four conductor system.

In this embodiment, a compensating capacitive device reduces an undesirable crosstalk signal (caused by a first mismatch between a plurality of mutual capacitive couplings associated with said four conductor system) when a processor controlling a switch connects the capacitive device between two conductors of a four conductor system.

A "***plurality of compensating capacitive devices***" is illustrated generally in figure 4 as the crosstalk compensator 200, which is described with particularity in the Specification at page 14, line 8 through page 15, line 16. Specific capacitive devices are illustrated in: figure 9 (reference numerals CC1-CC3, described with particularity in the Specification at page 24, line 26 through page 25, line 31); figure 10 (reference numerals CC1-CC3, described with particularity in the Specification at page 26, lines 6-31); figure 11 (reference numerals CC1-CC3, described with particularity in the Specification at page 27, line 6 through page 28, line 20); figure 12 (reference numerals CC1-CC*i*, described with particularity in the Specification

at page 28, line 23 through page 30, line 7); and figure 13 (reference numerals CC1-CC*i*, described with particularity in the Specification at page 30, line 10 through page 31, line 9).

A "***plurality of switches, each uniquely coupled to one of said capacitive devices***" for the above-described embodiments are illustrated in the figures 9-12. In figure 9, switches S1-S3 and processor based switch 250 are illustrated and are described with particularity in the Specification at page 24, line 31 through page 25, line 24. In figure 10, CC switcher 266 and line switcher 264 residing in the processor based switch 260 are illustrated and are described with particularity in the Specification at page 26, lines 6-22. In figure 11, CC switcher 276, line switcher 274 and detector 278 residing in the processor based switch 270 are illustrated and are described with particularity in the Specification at page 27, line 7 through page 28, line 9. In figure 12, three-way switches 288 and 290 residing in the first CC switcher 284 and the second CC switcher 286, respectively, and the detector 288 (which all reside in the processor based detector and switch 280) are illustrated and are described with particularity in the Specification at page 28, line 23 through page 29, line 21. In figure 13, capacitor compensating switches 310 and 312 residing in the first CC switcher 304 and the second CC switcher 306, respectively, and the detector 308 (which all reside in the processor based detector and switch 300) are illustrated and are described with particularity in the Specification at page 30, lines 10-33.

A "***processor controlling said switches***" is illustrated in: figure 9 (reference numeral 252, described with particularity in the Specification at page 24, line 33 through page 25, line 6); in figure 10 (reference numeral 262, described with particularity in the Specification at page 26, lines 10-11); figure 11 (reference numeral 272, described with particularity in the Specification at page 27, lines 11-13); figure 12 (reference numeral 282, described with

particularity in the Specification at page 28, lines 29-31); and figure 13 (reference numeral 302, described with particularity in the Specification at page 30, lines 10-18).

D. Summary of the Invention as defined by Independent Claim 37.

> 37. A system which reduces undesirable signals in a communication network, comprising:
>
> at least one compensating capacitive group;
>
> a plurality of compensating capacitive devices residing in each one of said at least one compensating capacitive group; and
>
> a plurality of compensating capacitive device switches, such that one of said plurality of compensating capacitive device switches is coupled to each one of said plurality of compensating capacitive devices,
>
> wherein said at least one compensating capacitive group is selectively connected in parallel with at least one pair of conductors selected from said plurality of parallel conductors, and wherein one of said at least one compensating capacitive device switches is actuated such that at least one of said plurality of compensating capacitive devices is switched such that a first mismatch between a plurality of mutual capacitive couplings associated with said plurality of conductors is reduced.

In this embodiment, at least one compensating capacitive group is selectively connected in parallel with at least one pair of conductors selected from a plurality of parallel conductors, wherein one of the compensating capacitive device switches are actuated such that at least one of the compensating capacitive devices are switched such that a first mismatch between a plurality of mutual capacitive couplings associated with the plurality of conductors is reduced.

At least one "***compensating capacitive group***" is illustrated generally in figure 4 as the crosstalk compensator 200, which is described with particularity in the Specification at page 14, line 8 through page 15, line 16. A more specific embodiment is illustrated in figures 5 and 6 (reference numeral 200), and is described with particularity in the Specification at page 15, line 19 through page 21, line 24. Other embodiments are disclosed in: figure 7 (reference numeral 201, described with particularity in the Specification at page 21, line 27

through page 23, line 17); figure 8 (reference numeral 202, described with particularity in the Specification at page 23, line 20 through page 24, line 23); figure 9 (reference numeral 203, described with particularity in the Specification at page 24, line 26 through page 25, line 31); figure 10 (reference numeral 204, described with particularity in the Specification at page 26, lines 6-31); figure 11 (reference numeral 205, described with particularity in the Specification at page 27, line 6 through page 28, line 20); figure 12 (reference numeral 206, described with particularity in the Specification at page 28, line 23 through page 30, line 7); and figure 13 (reference numeral 207, described with particularity in the Specification at page 30, line 10 through page 31, line 9).

A "***plurality of compensating capacitive devices" residing in each one of said at least one compensating capacitive group***" is illustrated generally in figure 4 as the crosstalk compensator 200, which is described with particularity in the Specification at page 14, line 8 through page 15, line 16. Specific capacitive devices are illustrated in: figure 6 (reference numerals CC1-CC6, described with particularity in the Specification at page 19, line 20 through page 20, line 22); figure 7 (reference numerals CC1-CC3, described with particularity in the Specification at page 21, lines 28-30); figure 8 (reference numerals CC1-CC3, described with particularity in the Specification at page 23, lines 20-24); figure 9 (reference numerals CC1-CC3, described with particularity in the Specification at page 24, line 26 through page 25, line 31); figure 10 (reference numerals CC1-CC3, described with particularity in the Specification at page 26, lines 6-31); figure 11 (reference numerals CC1-CC3, described with particularity in the Specification at page 27, line 6 through page 28, line 20); figure 12 (reference numerals CC1-CC*i*, described with particularity in the Specification at page 28, line 23 through page 30, line 7); and figure 13 (reference numerals CC1-CC*i*, described with particularity in the Specification at page 30, line 10 through page 31, line 9).

The plurality of compensating capacitive devices reside "in each one of said at least one compensating capacitive group."

A "plurality of ***compensating capacitive device switches***" are illustrated in the figures 6-12 by the switching devices. In figure 6, switches S1-S6 are illustrated and are described with particularity in the Specification at page 20, lines 7-22. In figure 7, switches S1-S3 and connection points 210 and 216 are illustrated and are described with particularity in the Specification at page 22, line 7 through page 23, line 17. In figure 8, switches S1-S3, SA and SB are illustrated and are described with particularity in the Specification at page 23, line 31 through page 24, line 15. In figure 9, switches S1-S3 and processor based switch 250 are illustrated and are described with particularity in the Specification at page 24, line 31 through page 25, line 24. In figure 10, CC switcher 266 and line switcher 264 residing in the processor based switch 260 are illustrated and are described with particularity in the Specification at page 26, lines 6-22. In figure 11, CC switcher 276, line switcher 274 and detector 278 residing in the processor based switch 270 are illustrated and are described with particularity in the Specification at page 27, line 7 through page 28, line 9. In figure 12, three-way switches 288 and 290 residing in the first CC switcher 284 and the second CC switcher 286, respectively, and the detector 288 (which all reside in the processor based detector and switch 280) are illustrated and are described with particularity in the Specification at page 28, line 23 through page 29, line 21. In figure 13, capacitor compensating switches 310 and 312 residing in the first CC switcher 304 and the second CC switcher 306, respectively, and the detector 308 (which all reside in the processor based detector and switch 300) are illustrated and are described with particularity in the Specification at page 30, lines 10-33. The switches are operated "such that one of said

plurality of compensating capacitive device switches is coupled to each one of said plurality of compensating capacitive devices."

E. Summary of the Invention as defined by Independent Claim 48.

> 48. A method which reduces undesirable signals in a communication network, comprising the steps of:
>
> connecting a compensating capacitive device group to a pair of conductors selected from said plurality of conductors;
>
> detecting a mismatch between said plurality of mutual coupling capacitances;
>
> selecting at least one compensating capacitive device residing in said compensating capacitive device group; and
>
> switching said at least one compensating capacitive device such that said at least one compensating capacitive device is connected in parallel with said pair of conductors such that said mismatch is reduced.

In this embodiment, a compensating capacitive device group is connected to a pair of conductors selected from the plurality of conductors, a mismatch is detected between the plurality of mutual coupling capacitances, at least one compensating capacitive device residing in the compensating capacitive device group is selected, and at least one compensating capacitive device is switched such that the compensating capacitive device is connected in parallel with the pair of conductors such that the mismatch is reduced.

"C***onnecting a compensating capacitive device group to a pair of conductors selected from said plurality of conductors***" is illustrated generally in figure 4 by the crosstalk compensator 200 coupled to two wire pairs (lines 1-2, and lines 3-4). The connecting is described with particularity in the Specification at page 14, line 8 through page 15, line 16. More specific embodiments are illustrated in figures 5 and 6 (reference numeral 200), and are described with particularity in the Specification at page 15, line 19 through page 21, line 24. Other embodiments are disclosed in: figure 7 (reference numeral 201, described with particularity in the Specification at page 21, line 27 through page 23, line 17); figure 8

(reference numeral 202, described with particularity in the Specification at page 23, line 20 through page 24, line 23); figure 9 (reference numeral 203, described with particularity in the Specification at page 24, line 26 through page 25, line 31); figure 10 (reference numeral 204, described with particularity in the Specification at page 26, lines 6-31); figure 11 (reference numeral 205, described with particularity in the Specification at page 27, line 6 through page 28, line 20); figure 12 (reference numeral 206, described with particularity in the Specification at page 28, line 23 through page 30, line 7); and figure 13 (reference numeral 207, described with particularity in the Specification at page 30, line 10 through page 31, line 9).

"***Detecting a mismatch between said plurality of mutual coupling capacitances***," in the embodiments illustrated in figures 6-10, is performed by the installer. In the embodiments illustrated in figures 11-13, the detecting is performed by detector 278, 288 and 308, respectively.

"***Selecting at least one compensating capacitive device residing in said compensating capacitive device group,***" in the embodiments illustrated in figures 6-10, is performed by the installer. In the embodiments illustrated in figures 11-13, the selecting is performed by processor 278, 288 and 308, respectively.

F. Summary of the Invention as defined by Independent Claim 48.

> 62. A computer readable medium having a program which reduces undesirable signals in a communication network the program comprising logic configured to perform the steps of:
>
> detecting a mismatch between said plurality of mutual coupling capacitances;
>
> selecting at least one compensating capacitive device residing in a compensating capacitive device group; and
>
> generating a switching instruction such that said at least one compensating capacitive device is connected in parallel with a pair of conductors such that said mismatch is reduced.

In this embodiment, "***Detecting a mismatch between said plurality of mutual coupling capacitances***" is performed by detector 278, 288 and 308, respectively (illustrated in figure 11 and described with particularity in the Specification at page 27, line 6 through page 28, line 20; illustrated in figure 12 and described with particularity in the Specification at page 28, line 29 through page 30, line 7; illustrated in figure 13 and described with particularity in the Specification at page 30, line 15 through page 31, line 9; and more generally described in the Specification at page 32, lines 29-34).

"***Selecting at least one compensating capacitive device residing in said compensating capacitive device group***" is performed by processor 278, 288 and 308, respectively (illustrated in figure 11 and described with particularity in the Specification at page 27, line 6 through page 28, line 20; illustrated in figure 12 and described with particularity in the Specification at page 28, line 29 through page 30, line 7; illustrated in figure 13 and described with particularity in the Specification at page 30, line 15 through page 31, line 9; and more generally described in the Specification at page 32, lines 29-34).

"***Generating a switching instruction such that said at least one compensating capacitive device is connected in parallel with a pair of conductors such that said mismatch is reduced***" is performed by processor 278, 288 and 308, respectively (illustrated in figure 11 and described with particularity in the Specification at page 27, line 6 through page 28, line 20; illustrated in figure 12 and described with particularity in the Specification at page 28, line 29 through page 30, line 7; illustrated in figure 13 and described with particularity in the Specification at page 30, line 15 through page 31, line 9; and more generally described in the Specification at page 32, lines 29-34).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-65 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Admitted prior art (Fig. 2) in view of *Sciacero et al.* (U.S. Patent 5,502,391), or *Arnett et al.* (U.S. Patents 6,186,834 or 6,176,742) and further in view of *Agazzi et al.* (U.S. Patent 4,669,116).

More particularly, in the stated rejection of independent claims 1, 33 and 37, the Final Office Action alleges that "the combination fails to teach selectively coupling by means of a relay or switch to the capacitive circuit" (referencing *Sciacero et al.* in combination with *Arnett* '742 or *Arnett* '834.) Then, the Final Office Action, at page 2 with respect to claims 1 and 38, and at pages 3-4 with respect to claim 33, alleges that "*Agazzi* teaches a non-linear cancellation of signals including echo or cross-talk in conjunction with data signals (see Col. 1 lines 17-20) by using a capacitive circuit with a plurality of capacitors in parallel which can be selectively activated by means of a relay in conjunction with a controller (see fig. 3)."

Additionally, independent claims 48 and 62 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over admitted prior art in view of *Sciacero*, *Arnett* '834 *or Arnett* '742, and further in view of *Agazzi*. More particularly, at page 4 of the Final Office Action, claim 48 is rejected by "the explanation as set forth regarding claim 1 because the system would perform the method steps." Also at page 4 of the Final Office Action, claim 62 is rejected by "the explanation as set forth regarding claim 1 because the system would perform the method steps by using a computer readable medium."

VII. ARGUMENT

A. Summary of Applicants' Argument

For the purposes of this Appeal, Applicants demonstrate that the proposed rejection relying on *Agazzi* is flawed because the teachings of *Agazzi* have been misapplied, and/or because *Agazzi* is an improper reference. Because the rejection of claims 1-65 under 35 U.S.C. §103(a) cannot be properly based upon *Agazzi*, the Final Office Action has failed to establish the requisite *prima facie* case of obviousness. Thus, claims 1-65 are not obvious under proposed combination of admitted prior art in view of *Sciacero*, *Arnett* '834 *or Arnett* '742, and further in view of *Agazzi*, and the rejection of the claims 1-65 should be withdrawn.

Applicants note that there may be separate grounds for patentability not argued herein, nor argued during prosecution of the instant application. To date, rejections in all Office Actions have improperly relied upon *Agazzi*. Applicants have repeatedly pointed out why *Agazzi* has been misapplied and why *Agazzi* is an improper reference. (Thus, Applicants have therefore not addressed other aspects of patentability in prior responses.) However, even in view of the Applicants' detailed arguments that *Agazzi* has been misapplied, and/or that *Agazzi* is an improper reference, the Final Office Action of April 4, 2004 maintains the rejection of claims 1-65 under 35 U.S.C. §103(a) using *Agazzi* as a cited reference. In maintaining the finality of the Final Office Action, no explanation is provided as to why *Agazzi* is still used as a reference in the rejection of claims 1-65 under 35 U.S.C. §103(a). Hence, Applicants must appeal herewith.

Applicants' first argument can be summarized as follows:

> a. *Agazzi* does not teach the technology alleged in the Office Action. That is, the teachings of *Agazzi* have been misapplied. Accordingly, because *Agazzi* fails to teach what is alleged, the proposed combination fails to teach, disclose or suggest the each and every limitation of the claimed invention. Accordingly, the rejection under the proposed combination fails since a *prima facie* case of obviousness is not established.

Alternatively, Applicants' second argument can be summarized as follows:

> b. *Agazzi* is not a proper reference upon which to base a rejection under 35 U.S.C. §103(a) because of a failure in the motivation to combine *Agazzi* with the other cited references. More particularly, *Agazzi* teaches away from the claimed embodiments of the invention in several respects, thereby demonstrating that there is no proper motivation to combine *Agazzi* with the other cited references. Accordingly, because *Agazzi* is not a proper reference upon which to base a rejection under 35 U.S.C. §103(a), the rejection fails since a *prima facie* case of obviousness is not established.

In either case, (*Agazzi* does not teach the alleged technology, or *Agazzi* is not a proper reference) these above-described reasons alone are sufficient for the Board to overturn the final rejection of claims 1-65.

B. *Agazzi* does not teach the technology alleged in the Final Office Action

The Final Office Action, at page 2, alleges that *Agazzi* "teaches a non-linear cancellation of signals including echo or cross-talk in conjunction with data signals in (see Col. 1 lines 17-20) by using a capacitive circuit with a plurality of capacitors in parallel which can be activated by means of a relay in conjunction with a controller in (see fig. 3)." Applicants maintain that the Final Office Action has misconstrued *Agazzi* for at least the reasons described below.

First, *Agazzi* *is limited* in its teachings of "non-linear cancellation of signals including echo **or cross-talk** in conjunction with data signals (see Col. 1 lines 17-20)" (emphasis added) as alleged by the Final Office Action. For the convenience of the Board, the section of *Agazzi* quoted in the Final Office Action is shown below:

> The purpose of an echo canceller is to remove the "near-end cross-talk" or "echo" signal which feeds through the hybrid into the local receiver, interfering with the data signal coming from a distant transmitter.

Although the phrase "near-end cross-talk" is briefly mentioned in *Agazzi*, a much closer inspection of *Agazzi* is required to determine if the reference to "cross-talk" in *Agazzi* corresponds to the cross-talk compensation provided by the present invention.

The purpose of *Agazzi* is to "provide an improved echo cancellation circuit and method which can correct for small amounts of non-linear distortion without a large complexity penalty or adaptation speed penalty" (Col. 1, lines 51-55). *Agazzi* discloses that "FIG. 1 depicts subscriber loop modems 10, 10' communicating on ***two wires*** 12" (emphasis added, Col. 2, lines 65-67). Nowhere in *Agazzi* is there any disclosure whatsoever of a second wire pair, or noise induced by other wires onto the *Agazzi* wires 12. Accordingly, Applicants respectfully point out that all teachings of *Agazzi* are ***limited*** to noise resulting from *communications over only the two wires* 12. [As compared to the cross-talk compensation provided by the present invention, which relates to a system wherein "mismatches in the mutual coupling capacitances in the customer's premises wiring system may give rise to undesirable levels of premises end crosstalk (PEXT) interference for which the preferred embodiment of the crosstalk compensator has been designed to mitigate by providing a system and method for the addition of compensating capacitors such that the mismatch is reduced or eliminated" (Application Specification page 10, lines 18-22)].

Closer inspection of *Agazzi* reveals that

> each modem circuit 10, 10' of FIG. 1 includes a transmitter 14, a hybrid circuit 16, ***echo canceller circuit 20***, summing circuit 18, and receiver 22. As will be described in more detail, each echo cancellation circuit 20 includes ***means to receive a first bit stream*** corresponding to a first transmitted data signal transmitted via transmitter 14 and hybrid circuit 16 over wires 12. Canceller 20 also includes ***means to receive a second transmitted data signal*** over wire 12. The second data signal ***includes an echo portion*** of the first bit stream having both linear and non-linear components. (Emphasis added, Col. 3, lines 1-11.)

Clearly, *Agazzi* is disclosing a system limited to communications over the two wires 12, and is silent about any type of cross-talk induced by another wire pair onto the *Agazzi* wires 12.

Agazzi discloses that "the echo canceller circuit 20 is typically implemented as a digital processor, since its input consists of an inherently digital bit stream" (Col. 3, lines 36-38). However, closer inspection is required to determine precisely the function of the "digital processor" in the *Agazzi* echo canceller circuit 20. *Agazzi* discloses two possible embodiments:

> In FIG. 2a, a purely digital echo canceller, using a front end A/D 34, is considered. S/H circuit 32 samples the second data signal at regular intervals and A/D 34 converts it to a digital format. ... Digital adaptive transversal circuit 30 generates a digital representation of the echo portion of the second data signal and digital circuit 36 provides means for subtracting the digital representation from the converted second data signal. (Col. 3, lines 49-52.)

> In FIG. 2b, the output of the echo canceller is converted to analog and the cancellation is performed in the analog domain. (Col. 3, lines 63-64.)

Accordingly, *Agazzi* employs *signal subtraction or cancellation* in either the digital or analog domains. *Agazzi* goes into further detail by disclosing

> in Section 2, a method of expanding an arbitrary nonlinear function of a number of bits in a series with a finite number of terms is presented. This expansion serves as the basis for the nonlinear echo canceller design procedures described later. Then in Section 3 the application of this expansion to multilevel transmitted signals, redundancies in the line code, and nonlinearities in the echo channel and the canceller itself are considered. Section 4 gives simulation results for the types of nonlinearities typically encountered in MOS D/A converters. These results indicate that, depending on the number of bits in the D/A converter, a 20 dB or greater increase in echo attenuation can be obtained by incorporating compensation for the D/A nonlinearity with a modest increase in canceller complexity. (Col. 4, lines 48-62.)

Accordingly, there is no express disclosure anywhere in this section of *Agazzi* of the use of any type of capacitive device to provide cross-talk compensation induced by another wire pair onto the *Agazzi* wires 12.

Arguably, *Agazzi* Fig. 3 does illustrate elements that may be construed as a capacitor circuit. However, *Agazzi* fails to disclose any functionality associated with the capacitors of Fig. 3. *Agazzi* is limited to teaching, with respect to Fig. 3, that:

> an alternative solution to the problem in which the transversal filter summation is done by analog circuitry and thus the adaptation can compensate for the D/A nonlinearity is shown in FIG. 3 and has also been demonstrated. (Details of the above are described in more detail in the cross-referenced application entitled "Echo Canceller Tolerant of Non-Linear Elements", Ser. No. 414,515, filed Sept. 2, 1982.) However, that solution cannot correct other sources of distortion, like pulse asymmetry or saturation in transformers. (Col. 4, lines 17-27.)

Accordingly, there is no express teaching whatsoever regarding the functionality of the *Agazzi* capacitors illustrated in Fig. 3. Any such conclusion regarding the functionality of the *Agazzi* capacitors illustrated in Fig. 3 made by the Final Office Action must be based upon assumptions not supported by documentary evidence.

Agazzi Fig. 10 additionally illustrates elements that may be construed as a capacitor circuit. However, *Agazzi* fails to disclose any functionality associated with the capacitors of Fig. 10. *Agazzi* is limited to teaching, with respect to Fig. 10, that:

> in order to make the numerical examples realistic, assume the D/A converter is to be implemented in MOS technology using the technique shown in FIG. 10. The four most significant bits are provided by a string of 16 diffused resistors and the remaining bits (from 6 to 9 in simulations) by a binary weighted capacitor array. Because of diffusion concentration gradients, voltage coefficient, and photolithographic mismatches, the resistors cannot be guaranteed to be equal to within one LSB unless laser trimming is used. Thus, in the absence of trimming, a nonlinear transfer characteristic results. This nonlinearity can have a systematic component due to concentration gradients, and a random component due to photolithographic mismatches. (Col. 17, lines 5-17.)

Accordingly, there is no express teaching that the capacitors illustrated in Fig. 10 provide compensation. Any conclusions that the capacitors illustrated in Fig. 10 provide compensation made by the Final Office Action must be based upon assumptions not supported by documentary evidence.

Finally, the equations of *Agazzi* section 3 (Application to Echo Cancellation) employ a term C_k. However, *this term **does not** relate to capacitance. Agazzi* expressly teaches that "C_k is the current transmitted data symbol" (Col. 8, lines 62-63). Therefore, *Agazzi* does not disclose, teach or suggest that any type of capacitance that is used for compensation of any type of cross-talk compensation induced by another wire pair onto the *Agazzi* wires 12.

The Final Office Action, at page 2, then alleges that *Agazzi* "teaches a non-linear cancellation of signals including echo or cross-talk in conjunction with data signals in (see Col. 1 lines 17-20) ***by*** **using a capacitive circuit** with a **plurality of capacitors** in parallel which **can be activated by means of a relay in conjunction with a controller** in (see fig. 3)" (emphasis added). The above characterization of *Agazzi* is not correct, for at least the reasons described below. First, the illustrated capacitive circuit of *Agazzi* Fig. 3, even though it does appear to illustrate a plurality of capacitors, ***is not disclosed as being used for cancellation of cross-talk***, as implied in the Final Office Action. The Examiner is respectfully referred to the sections above which clearly demonstrate that *Agazzi* discloses ***nothing*** with respect to the functionality of the capacitors in *Agazzi* Fig. 3 (or in *Agazzi* Fig. 10). Accordingly, the Final Office Action must necessarily infer the alleged functionality of the *Agazzi* capacitors of Fig. 3 based on assumptions not supported by documentary evidence. Applicants maintain that it is improper for the Final Office Action to conclude that the functionality of the capacitors in *Agazzi* Fig. 3 (or in *Agazzi* Fig. 10) performs "a non-linear cancellation of signals including echo or cross-talk" because *Agazzi* simply does not support such a conclusion.

Second, *Agazzi* teaches nothing with respect to cross-talk induced by another wire pair onto a first wire pair (the *Agazzi* wires 12) through mutual coupling since *Agazzi* is limited to a two wire system. Accordingly, Applicants maintain that it is improper for the Final Office Action to conclude such functionality of the capacitors in *Agazzi* Fig. 3 (or in *Agazzi* Fig. 10).

Agazzi simply does not support such a conclusion. That is, since *Agazzi* teaches nothing about mutual coupling between multiple pairs of conductors (because *Agazzi* is limited to a two wire system), it is improper for the Final Office Action to conclude that *Agazzi* "teaches a non-linear cancellation of signals including echo or ***cross-talk*** in conjunction with data signals in (see Col. 1 lines 17-20) **by using a capacitive circuit** with a **plurality of capacitors** in parallel which can be activated by means of a relay in conjunction with a controller in (see fig. 3)."

Finally, the Final Office Action, at page 2, alleges that *Agazzi* "teaches a non-linear cancellation of signals including echo or cross-talk in conjunction with data signals in (see Col. 1 lines 17-20) by using a capacitive circuit with a plurality of capacitors in parallel which **can be activated by means of a relay in conjunction with a controller** in (see fig. 3)." This allegation improperly implies that the *Agazzi* capacitive circuit is activated by relays in conjunction with a controller *so that the capacitors may cancel cross-talk. Agazzi* is limited to disclosing, with respect to Fig. 3, the phrase "SHR = SWITCH CONTROL LOGIC" which is used to label the block (wherein the data enters the echo canceller configuration illustrated in Fig. 3), and is limited to disclosing by illustration switches coupled to the illustrated capacitors. This phrase "SHR = SWITCH CONTROL LOGIC" does not, by itself, teach, disclose or suggest that *Agazzi* "teaches a non-linear cancellation of signals including echo or cross-talk in conjunction with data signals in (see Col. 1 lines 17-20) by using a capacitive circuit with a plurality of capacitors in parallel which **can be activated by means of a relay in conjunction with a controller** in (see fig. 3)," as alleged in the Final Office Action at page 2. That is, *Agazzi* simply does not support the conclusion of the Final Office Action that the capacitors are switched by a controller to compensate for cross-talk. If the Final Office Action is making assumptions about the purpose, functionality and operation of the block labeled with the phrase

"SHR = SWITCH CONTROL LOGIC" in Fig. 3, such assumptions are improper because such assumptions are not supported by documentary evidence.

The detailed description of Fig. 3 does not support the allegation of the Final Office Action that the *Agazzi* capacitors illustrated in Fig. 3 are switched by a controller for "non-linear cancellation of signals including echo or cross-talk in conjunction with data signals in (see Col. 1 lines 17-20) by using a capacitive circuit with a plurality of capacitors in parallel which **can be activated by means of a relay in conjunction with a controller** in (see fig. 3)." The entire text of *Agazzi* regarding FIG. 3 is printed below for the convenience of the Examiner:

> An alternative solution to the problem in which the transversal filter summation is done by analog circuitry and thus the adaptation can compensate for the D/A nonlinearity is shown in FIG. 3 and has also been demonstrated. (Details of the above are described in more detail in the cross-referenced application entitled "Echo Canceller Tolerant of Non-Linear Elements", Ser. No. 414,515, filed Sept. 2, 1982.) However, that solution cannot correct other sources of distortion, like pulse asymmetry or saturation in transformers. (Col. 4, lines 17-27.)

As apparent from the text above, there is no teaching to support a conclusion that there is "cancellation of ... cross-talk ... by using a capacitive circuit with a plurality of capacitors in parallel which can be activated by means of a relay in conjunction with a controller in (see fig. 3)" as alleged by the Final Office Action.

However, the Detailed Description of *Agazzi* does include limited discussion of switches elsewhere. The Examiner is respectfully referred to *Agazzi* from Col. 5, line 60 through Col. 6, line 31. In this section of *Agazzi*, the use of a "tree of switches 52 and adders 50" and "switches 54" are disclosed. These references are not to any switches illustrated in Figs. 3 or 10. There are no other disclosures regarding the use of other switches anywhere in *Agazzi* (and more particularly, to the switches illustrated in *Agazzi* Figs. 3 or 10). Clearly, this section ***does not*** show that *Agazzi* "teaches a non-linear cancellation of signals including echo or cross-talk in

conjunction with data signals in (see Col. 1 lines 17-20) by using a capacitive circuit with a plurality of capacitors in parallel which **can be activated by means of a relay in conjunction with a controller** in (see fig. 3)" as alleged in the Final Office Action.

Summarizing, *Agazzi* is silent about any type of cross-talk induced by another wire pair onto the *Agazzi* wires 12. Such a form of cross-talk ***is not contemplated anywhere*** in *Agazzi* because *Agazzi* is limited to a single wire pair (wires 12). *Agazzi* does not teach, disclose or suggest anything regarding the functionality of the capacitors illustrated in Figs. 3 or 10. In fact, *Agazzi* does not disclose, teach or suggest that any type of capacitance is used for compensation of any type of cross-talk compensation *induced by another wire pair onto the Agazzi wires 12*. Any such functionality of the capacitors must be improperly inferred based upon assumptions that are not supported by documentary evidence. Finally, *Agazzi* does not disclose, teach or suggest capacitor switching by a controller for any purpose whatsoever. (*Agazzi* is limited to disclosing a block labeled with the phrase "SHR = SWITCH CONTROL LOGIC" in Fig. 3, and is limited to illustrating switches in Figs. 3 and 10.) To conclude that the *Agazzi* capacitors are switched by a relay *to compensate for cross-talk noise* is improper because such a conclusion must be inferred by the Final Office Action based upon assumptions that are not supported by documentary evidence. Accordingly, Applicants maintain that the Final Office Action has misconstrued *Agazzi*, and that the allegation that *Agazzi* "teaches a non-linear cancellation of signals including echo or cross-talk in conjunction with data signals in (see Col. 1 lines 17-20) by using a capacitive circuit with a plurality of capacitors in parallel which can be activated by means of a relay in conjunction with a controller in (see fig. 3)" is not supportable.

Given that the Final Office Action has misconstrued *Agazzi*, and that the Final Office Action allegation is not supportable, the proposed combination of admitted prior art in view of *Sciacero*, *Arnett* '834 or *Arnett* '742, and further in view *Agazzi* fails to teach, disclose or

suggest every limitation of the claimed invention. That is, the basis of the rejection is fundamentally flawed.

Accordingly, because *Agazzi* fails to teach what is alleged, the proposed combination fails to teach, disclose or suggest the each and every limitation of the claimed invention. Since each and every limitation of the rejected claims 1-65 are not taught, disclosed or suggested in the proposed combination of references used in the Final Office Action to reject claims 1-65, for this reason alone, the requisite *prima facie* case of establishing obviousness has not been made. Thus, claims 1-65 are not obvious under proposed combination, and the rejection of the claims 1-65 should be withdrawn.

C. *Agazzi* is not a proper reference

Applicants maintain that *Agazzi* is not a proper reference upon which to base a rejection under 35 U.S.C. §103(a) because of a failure in the motivation to combine *Agazzi* with the other cited references. More particularly, *Agazzi* teaches away from the claimed embodiments of the invention in several respects, thereby demonstrating that there is no proper motivation to combine *Agazzi* with the other cited references. Accordingly, because *Agazzi* is not a proper reference upon which to base a rejection under 35 U.S.C. §103(a), the rejection fails since a *prima facie* case of obviousness is not established..

The Final Office Action, at page 2, concludes that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Agazzi into that of the combination." Applicants respectfully traverse this conclusion and assert that (a) there is no teaching or suggestion to combine *Agazzi* with the admitted prior art (Fig. 2) in view of *Sciacero*, *Arnett* '834 or *Arnett* '835, (b) the present application and pending claims have clearly been used as a road map and template to combine the foregoing

teachings, and (c) it is clear that none of these references appreciated the advantages of the present invention. More particularly, for at least the reasons detailed below, *Agazzi* ***teaches away*** from the present invention in several aspects. These several teachings in *Agazzi* demonstrate that one skilled in the art would not be motivated to combine *Agazzi* with the other proposed references.

First, *Agazzi* ***teaches away*** from the present invention because *Agazzi* is limited to disclosing compensation for a two wire system. *Agazzi* discloses that "FIG. 1 depicts subscriber loop modems 10,10' communicating on ***two wires*** 12" (emphasis added, Col. 2, lines 65-67). Nowhere in *Agazzi* is there any disclosure whatsoever of a second wire pair, or noise induced by other wires onto the *Agazzi* wires 12. Applicants respectfully point out that all teachings of *Agazzi* are ***limited*** to noise resulting from *communications over only the two wires* 12. [As compared to the cross-talk compensation provided by the present invention, which relates to a system wherein "mismatches in the mutual coupling capacitances in the customer's premises wiring system may give rise to undesirable levels of premises end crosstalk (PEXT) interference for which the preferred embodiment of the crosstalk compensator has been designed to mitigate by providing a system and method for the addition of compensating capacitors such that the mismatch is reduced or eliminated" (Application Specification page 10, lines 18-22)]. Therefore, one skilled in the art would not look to *Agazzi* for compensating mismatches in the mutual coupling capacitances between multiple pairs of wires because *Agazzi* ***is limited*** to disclosing compensation for a two wire system. That is, *Agazzi* teaches away from the present invention because *Agazzi* ***is limited*** to disclosing compensation for a two wire system and because *Agazzi* purposely avoids discussion of cross-talk induced by other wire pairs.

Second, *Agazzi* ***teaches away*** from the present invention because *Agazzi* employs *signal subtraction or cancellation* in either the digital or analog domains. *Agazzi* discloses that:

> the echo canceller circuit 20 is typically implemented as a digital processor, since its input consists of an inherently digital bit stream (Col. 3, lines 36-38).

However, closer inspection is required to determine precisely the function of the "digital processor" in the *Agazzi* echo canceller circuit 20. *Agazzi* discloses two possible embodiments.

> In FIG. 2a, a purely digital echo canceller, using a front end A/D 34, is considered. S/H circuit 32 samples the second data signal at regular intervals and A/D 34 converts it to a digital format. ... Digital adaptive transversal circuit 30 generates a digital representation of the echo portion of the second data signal and digital circuit 36 provides means for subtracting the digital representation from the converted second data signal. (Col. 3, lines 49-52.), and
>
> In FIG. 2b, the output of the echo canceller is converted to analog and the cancellation is performed in the analog domain. (Col. 3, lines 63-64.)

Accordingly, because *Agazzi* is limited to employing signal subtraction or cancellation in either the digital or analog domains, one skilled in the art would not look to *Agazzi* for compensating mismatches in the mutual coupling capacitances between multiple pairs of wires. That is, *Agazzi* teaches away from the present invention because *Agazzi* ***is limited*** to disclosing compensation by signal subtraction or cancellation in either the digital or analog domains.

Third, *Agazzi* ***teaches away*** from the present invention because *Agazzi* fails to disclose, teach or suggest anywhere *the use of* ***capacitors*** to compensate for cross-talk noise. Arguably, *Agazzi* Fig. 3 does illustrate elements that may be construed as a capacitor circuit. However, *Agazzi* fails to disclose any functionality associated with the capacitors of Fig. 3. *Agazzi* is limited to teaching, with respect to Fig. 3, that:

> an alternative solution to the problem in which the transversal filter summation is done by analog circuitry and thus the adaptation can compensate for the D/A nonlinearity is shown in FIG. 3 and has also been demonstrated. (Details of the above are described in more detail in the cross-referenced application entitled 'Echo Canceller Tolerant of Non-Linear Elements', Ser. No. 414,515, filed Sept. 2, 1982.) However, that solution cannot correct other sources of distortion, like pulse asymmetry or saturation in transformers. (Col. 4, lines 17-27.)

Accordingly, there is no express teaching whatsoever regarding the functionality of the *Agazzi* capacitors illustrated in Fig. 3. *Agazzi* Fig. 10 additionally illustrates elements that may be construed as a capacitor circuit. However, *Agazzi* fails to disclose any functionality associated with the capacitors of Fig. 10. *Agazzi* is limited to teaching, with respect to Fig. 10, that:

> in order to make the numerical examples realistic, assume the D/A converter is to be implemented in MOS technology using the technique shown in FIG. 10. The four most significant bits are provided by a string of 16 diffused resistors and the remaining bits (from 6 to 9 in simulations) by a binary weighted capacitor array. Because of diffusion concentration gradients, voltage coefficient, and photolithographic mismatches, the resistors cannot be guaranteed to be equal to within one LSB unless laser trimming is used. Thus, in the absence of trimming, a nonlinear transfer characteristic results. This nonlinearity can have a systematic component due to concentration gradients, and a random component due to photolithographic mismatches. (Col. 17, lines 5-17.)

Accordingly, because *Agazzi* completely fails to disclose any functionality of the capacitors illustrated in *Agazzi* Figs. 3 or 10, and in particular fails to disclose using the capacitors to compensate mismatches in the mutual coupling capacitances in the customer's premises wiring system, one skilled in the art would not look to *Agazzi* providing such compensation in accordance with the present invention. That is, *Agazzi* teaches away from the present invention because *Agazzi* fails to disclose, teach or suggest anywhere the use of capacitors to compensate for cross-talk noise.

Applicants have detailed above three reasons why *Agazzi* teaches away from the present invention. These reasons, alone or in combination, clearly demonstrate that one skilled in the

art would not look to *Agazzi* for providing compensation in accordance with the present invention. Accordingly, *Agazzi* cannot be properly combined with the admitted prior art (Fig. 2) in view of *Sciacero*, *Arnett* '834 or *Arnett* '835. Since *Agazzi* is not properly combinable with the references cited in the Final Office Action, a *prima facie* case establishing an obviousness rejection cannot be established using *Agazzi* as a reference. Accordingly, claims 1-65 are not obvious under proposed combination and the rejection should be withdrawn for at least this reason alone.

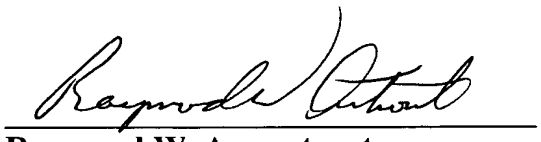
VIII. CONCLUSION

Since the proposed rejection relying on *Agazzi* is flawed (because the teachings of *Agazzi* have been misapplied, and/or because *Agazzi* is an improper reference), the rejection of claims 1-65 under 35 U.S.C. §103(a) cannot be properly based upon *Agazzi*. Accordingly, the Final Office Action has failed to establish the requisite *prima facie* case of obviousness. Thus, claims 1-65 are not obvious under proposed combination of admitted prior art in view of *Sciacero*, *Arnett* '834 *or Arnett* '742, and further in view of *Agazzi*, and the rejection of the claims 1-65 should be withdrawn.

In view of the foregoing, it is believed that all pending claims 1-65 are in proper condition for allowance, and the Board is respectfully requested to overturn the Examiner's final rejections of claims 1-65.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor are hereby authorized to be charged to Deposit Account No. 16-0255.

Respectfully submitted,
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.



Raymond W. Armentrout
Registration No. 45,866

100 Galleria Parkway, Suite 1750
Atlanta, Georgia 30339-5948
770-933-9500

IX. APPENDIX A

Claims Currently Pending

1. (Original) A system for reducing undesirable signals in a communication network, comprising:

means for compensating, said compensating means providing capacitance;

means for connecting said compensating means to a pair of conductors selected from a plurality of conductors; and

means for selectively actuating said compensating means such that said compensating means, when actuated by said actuating means, reduces an undesirable crosstalk signal caused by a mismatch between a plurality of mutual capacitive couplings associated with said plurality of conductors.

2. (Original) The system of claim 1, wherein said compensating means comprises a compensating capacitive device, wherein said actuating means actuates said compensating capacitive device such that said compensating capacitive device is connected in parallel with said pair of conductors to reduce said mismatch.

3. (Original) The system of claim 2, wherein said compensating means comprises a plurality of compensating capacitive devices, wherein said means for selectively actuating selects two or more of said plurality of compensating capacitive devices such that said selected compensating capacitive devices are connected in parallel with said pair of conductors to reduce said mismatch.

4. (Original) The system of claim 3, wherein at least one of said plurality of compensating capacitive devices is a capacitor.

5. (Original) The system of claim 3, wherein at least one of said plurality of compensating capacitive devices is a varactor.

6. (Original) The system of claim 3, further comprising a means for detection wherein said detection means detects said mismatch, and further comprising a means for

determination, wherein said determination means instructs said actuating means such that said mismatch is reduced.

7. (Original) The system of claim 6, wherein said mismatch is reduced to at least a predefined threshold.

8. (Original) The system of claim 2, further comprising a second means for compensating, said second compensating means connected to a second pair of conductors selected from said plurality of conductors by said connecting means, such that when said second compensation means is actuated by said actuating means, said second compensation means reduces said undesirable crosstalk signal caused by a second mismatch between a plurality of mutual capacitive couplings associated with said plurality of conductors.

9. (Original) The system of claim 8, wherein said second compensating means comprises a second compensating capacitive device, wherein said actuating means actuates said second compensating capacitive device such that said second compensating capacitive device is connected in parallel with said second one pair of conductors to reduce said second mismatch.

10. (Original) The system of claim 9, wherein said second compensating means comprises a second plurality of compensating capacitive devices, wherein said actuating means selects two or more of said second plurality of compensating capacitive devices such that said selected compensating capacitive devices are connected in parallel with said second pair of conductors to reduce said second mismatch.

11. (Original) The system of claim 10, wherein at least one of said second plurality of compensating capacitive devices is a capacitor.

12. (Original) The system of claim 10, wherein at least one of said second plurality of compensating capacitive devices is a varactor.

13. (Original) The system of claim 10, further comprising a means for detection wherein said detection means detects said second mismatch, and further comprising a means for determination, wherein said determination means instructs said actuating means such that said second mismatch is reduced.

14. (Original) The system of claim 13, wherein said second mismatch is reduced to at least a second predefined threshold.

15. (Original) The system of claim 8, further comprising a third means for compensating, said third compensating means connected to a third pair of conductors selected from said plurality of conductors by said connecting means, such that when said third compensation means is actuated by said actuating means, said third compensation means reduces said undesirable crosstalk signal caused by a third mismatch between a plurality of mutual capacitive couplings associated with said plurality of conductors.

16. (Original) The system of claim 15, wherein said third compensating means comprises a third compensating capacitive device, wherein said actuating means actuates said third compensating capacitive device such that said third compensating capacitive device is connected in parallel with said third one pair of conductors to reduce said third mismatch.

17. (Original) The system of claim 16, wherein said third compensating means comprises a third plurality of compensating capacitive devices, wherein said actuating means selects two or more of said third plurality of compensating capacitive devices such that said selected compensating capacitive devices are connected in parallel with said third pair of conductors to reduce said third mismatch.

18. (Original) The system of claim 17, wherein at least one of said third plurality of compensating capacitive devices is a capacitor.

19. (Original) The system of claim 17, wherein at least one of said third plurality of compensating capacitive devices is a varactor.

20. (Original) The system of claim 17, further comprising a means for detection wherein said detection means detects said third mismatch, and further comprising a means for determination, wherein said determination means instructs said actuating means such that said third mismatch is reduced.

21. (Original) The system of claim 20, wherein said third mismatch is reduced to at least a third predefined threshold.

22. (Original) The system of claim 20, wherein said means for determination determines instructions to instruct said actuating means to concurrently reduce said mismatch, said second mismatch, said third mismatch and a fourth mismatch, said fourth mismatch arising between a plurality of mutual capacitive couplings associated with said plurality of conductors.

23. (Original) The system of claim 1, further comprising:

a plurality of means for compensating;

means for detecting, such that said detecting means detects a plurality of mismatches arising between a plurality of conductors; and

means for determination, wherein said determination means instructs said actuating means to actuate said plurality of compensating means such that said plurality of mismatches are reduced.

24. (Original) The system of claim 23, wherein said plurality of mismatches are compensated to zero.

25. (Original) The system of claim 1, further comprising:

more than four means for compensating;

means for detecting, such that said detecting means detects more than four mismatches arising between a plurality of conductors; and

means for determination, wherein said determination means instructs said actuating means to actuate said more than four compensating means such that said more than four mismatches are reduced.

26. (Original) The system of claim 1, wherein said means for compensating comprises more than four compensating capacitive devices, and further comprising:

means for detecting, such that said detecting means detects more than four mismatches arising between a plurality of conductors; and

means for determination, wherein said determination means instructs said actuating means to actuate at least four of said compensating capacitive devices such that said more than four mismatches are reduced.

27. (Original) The system of claim 26, wherein at least one of said four compensating capacitive devices is a capacitor.

28. (Original) The system of claim 26, wherein at least one of said four compensating capacitive devices is a varactor.

29. (Original) The system of claim 1, wherein said plurality of conductors are subscriber loops carrying a plurality of communication signals, and wherein said plurality of communication signals are transmitting at substantially the same frequency.

30. (Original) The system of claim 1, wherein said mismatches between said plurality of mutual capacitive coupling means are produced in a customer premises wiring system.

31. (Original) The system of claim 2, wherein said compensating means further includes a compensating resistive element residing in at least one of said plurality of compensating capacitive devices.

32. (Original) The system of claim 2, wherein said compensating means further includes a compensating inductive element residing in at least one of said plurality of compensating capacitive devices.

33. (Previously presented) A system for reducing undesirable signals in a communication network, comprising:

a plurality of compensating capacitive devices;

a plurality of switches, each uniquely coupled to one of said capacitive devices; and

a processor controlling said switches,

such that when at least one of said switches are actuated by said processor, said corresponding compensating capacitive device is connected between two conductors of a four conductor system, such that said compensating capacitive device reduces an undesirable crosstalk signal caused by a first mismatch between a plurality of mutual capacitive couplings associated with said four conductor system.

34. (Original) The system of claim 33, wherein at least one of said plurality of compensating capacitive devices is a capacitor.

35. (Original) The system of claim 33, wherein at least one of said plurality of compensating capacitive devices is a varactor.

36. (Original) The system of claim 33, wherein said undesirable crosstalk signal is reduced to a predefined threshold.

37. (Original) A system which reduces undesirable signals in a communication network, comprising:

at least one compensating capacitive group;

a plurality of compensating capacitive devices residing in each one of said at least one compensating capacitive group; and

a plurality of compensating capacitive device switches, such that one of said plurality of compensating capacitive device switches is coupled to each one of said plurality of compensating capacitive devices,

wherein said at least one compensating capacitive group is selectively connected in parallel with at least one pair of conductors selected from said plurality of parallel conductors, and wherein one of said at least one compensating capacitive device switches is actuated such that at least one of said plurality of compensating capacitive devices is switched such that a first

mismatch between a plurality of mutual capacitive couplings associated with said plurality of conductors is reduced.

38. (Original) The system of claim 37, wherein at least one of said plurality of compensating capacitive devices is a capacitor.

39. (Original) The system of claim 37, wherein at least one of said plurality of compensating capacitive devices is a varactor.

40. (Original) The system of claim 37, further comprising a plurality of line switches coupled to said at least one compensating capacitive device group such that said at least one compensating capacitive group is selectively connected to said pair of conductors.

41. (Original) The system of claim 40, further comprising a processor such that said processor processes at least one line switching instruction and configures each one of said line switches according to said at least one line switching instruction.

42. (Original) The system of claim 41, further comprising a detector configured to detect said at least one mismatch and configured to transmit data corresponding to said at least one mismatch to said processor, and wherein said processor determines said at least one line switching instruction.

43. (Original) The system of claim 37, further comprising a processor such that said processor processes at least one compensating capacitive device switching instruction and configures each one of said compensating capacitive device switches according to said at least one compensating capacitive device switching instruction.

44. (Original) The system of claim 43, further comprising a detector configured to detect said at least one mismatch and configured to transmit data corresponding to said at least one mismatch to said processor, and wherein said processor determines said at least one compensating capacitive device switching instruction.

45. (Original) The system of claim 37, wherein said communication network is a subscriber loop communication network transmitting a plurality of digital data signals over a plurality of subscriber loops.

46. (Original) The system of claim 45, wherein said plurality of digital data signals are transmitted at substantially the same frequency.

47. (Original) The system of claim 37, wherein said at least one mismatch is produced in a customer premises wiring system.

48. (Original) A method which reduces undesirable signals in a communication network, comprising the steps of:

connecting a compensating capacitive device group to a pair of conductors selected from said plurality of conductors;

detecting a mismatch between said plurality of mutual coupling capacitances;

selecting at least one compensating capacitive device residing in said compensating capacitive device group; and

switching said at least one compensating capacitive device such that said at least one compensating capacitive device is connected in parallel with said pair of conductors such that said mismatch is reduced.

49. (Original) The system of claim 48, wherein at least one of said plurality of compensating capacitive devices is a capacitor.

50. (Original) The system of claim 48, wherein at least one of said plurality of compensating capacitive devices is a varactor.

51. (Original) The method of claim 48, wherein said mismatch is reduced to at least a predefined threshold.

52. (Original) The method of claim 48, future including the steps of:

connecting a second compensating capacitive device group to a second pair of conductors selected from said plurality of conductors;

detecting a second mismatch between said plurality of mutual coupling capacitances;

selecting at least one compensating capacitive device residing in said second compensating capacitive device group; and

switching said at least one compensating capacitive device residing in said second compensating capacitive device group such that said at least one compensating capacitive device residing in said second compensating capacitive device group is connected in parallel with said second pair of conductors such that said second mismatch is reduced.

53. (Original) The system of claim 52, wherein at least one of said plurality of compensating capacitive devices is a capacitor.

54. (Original) The system of claim 52, wherein at least one of said plurality of compensating capacitive devices is a varactor.

55. (Original) The method of claim 52, wherein said second mismatch is reduced to at least a second predefined threshold.

56. (Original) The method of claim 48, future including the steps of:

connecting a third compensating capacitive device group to a third pair of conductors selected from said plurality of conductors;

detecting a third mismatch between said plurality of mutual coupling capacitances;

selecting at least one compensating capacitive device residing in said third compensating capacitive device group; and

switching said at least one compensating capacitive device residing in said third compensating capacitive device group such that said at least one compensating capacitive device residing in said third compensating capacitive device group is connected in parallel with said third pair of conductors such that said third mismatch is reduced.

57. (Original) The system of claim 56, wherein at least one of said plurality of compensating capacitive devices is a capacitor.

58. (Original) The system of claim 56, wherein at least one of said plurality of compensating capacitive devices is a varactor.

59. (Original) The method of claim 56, wherein said third mismatch is reduced to at least a third predefined threshold.

60. (Original) The method of claim 56, wherein the steps of selecting and switching concurrently reduces said mismatch, said second mismatch, said third mismatch and a fourth mismatch, said fourth mismatch arising between a plurality of mutual capacitive couplings associated with said plurality of conductors.

61. (Original) The method of claim 60, wherein the selecting and switching concurrently zeros out said mismatch, said second mismatch, said third mismatch and a fourth mismatch, said fourth mismatch arising between a plurality of mutual capacitive couplings associated with said plurality of conductors.

62. (Original) A computer readable medium having a program which reduces undesirable signals in a communication network the program comprising logic configured to perform the steps of:

detecting a mismatch between said plurality of mutual coupling capacitances;

selecting at least one compensating capacitive device residing in a compensating capacitive device group; and

generating a switching instruction such that said at least one compensating capacitive device is connected in parallel with a pair of conductors such that said mismatch is reduced.

63. (Original) The computer readable medium of claim 62, further comprising logic configured to perform the steps of:

detecting a second mismatch between said plurality of mutual coupling capacitances;

selecting at least one compensating capacitive device residing in a second compensating capacitive device group; and

generating a switching instruction such that said at least one compensating capacitive device residing in said second compensating capacitive device group is connected in parallel with a second pair of conductors such that said second mismatch is reduced.

64. (Original) The computer readable medium of claim 62, further comprising logic configured to perform the steps of:

detecting a third mismatch between said plurality of mutual coupling capacitances;

selecting at least one compensating capacitive device residing in a third compensating capacitive device group; and

generating a switching instruction such that said at least one compensating capacitive device residing in said third compensating capacitive device group is connected in parallel with a third pair of conductors such that said third mismatch is reduced.

65. (Original) The computer readable medium of claim 62, further comprising logic configured to perform the steps of selecting and generating concurrently reduces said mismatch, said second mismatch, said third mismatch and a fourth mismatch, said fourth mismatch arising between a plurality of mutual capacitive couplings associated with said plurality of conductors.